MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2, 2016/2017 SESSION

ECE 3226 - ADVANCED COMPUTER ARCHITECTURE AND PARALLEL COMPUTING

(CE)

24 FEB 2017
03:00 P.M – 05:00 P.M
(2 Hours)

INSTRUCTIONS TO STUDENT

1. This question paper consists of five (5) pages only (including this page).
2. There are **FOUR (4) QUESTIONS** in this paper. Answer **ALL QUESTIONS**. All questions carry 25 marks each.
3. Write your answers in the Answer Booklet provided.

Question 1

a) In computing, MIMD (multiple instruction multiple data) is a technique employed to achieve parallelism. There are two models of memory used in MIMD architecture. Illustrate and explain the models with diagrams.

[6 marks]

b) A particular program runs in 10 seconds on computer A, which has a 4 GHz clock. We are trying to help a computer engineer to build a computer, B, which will run this program in 6 seconds. The engineer has determined that a substantial increase in the clock rate is possible, but this increase will affect the rest of PU design, causing computer B to require 1.2 times as many clock cycles as computer A for this program.

i. Calculate CPU clock cycles for computer A

[4 marks]

ii. Calculate clock rate for computer B

[5 marks]

c) In a data acquisition process, experiment is launched and suppose we have made the following measurements:

Frequency of floating-point (FP) operations = 25%
Average CPI of floating-point operations = 4.0
Average CPI for other instructions = 1.33
Frequency of floating-point square root (FPSQR) = 2% , this 2% is a subset of floating point operation.
CPI for FPSQR = 20

Assume that the two design alternatives:
Design 1: Decrease the original CPI of FPSQR to 2.
Design 2 : Decrease the average original CPI to all FP operations to 2.5.

i. Calculate the original CPI with no enhancement. [2 marks]

ii. Calculate the new CPI on Design 1. [2 marks]

iii. Calculate the new CPI on Design 2. [2 marks]

iv. Compare the two design alternatives from Design 1 and Design 2 using the processor performance equation.

[4 marks]

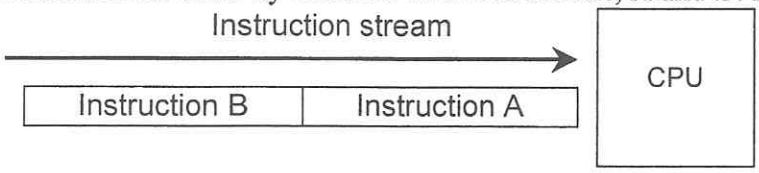
Continued .....

Question 2

a) In computers, a pipeline is the continuous and overlapped movement of instruction to the processor or in the arithmetic steps taken by processor to perform an instruction. Pipelines are usually divided into two classes. Illustrate and explain these two classes.

[6 marks]

b) There are 3 types of data hazards, which can be classified based on the order of read and write accesses in the instructions. Name the three types of data hazard and illustrate them by consider two instructions, A and B. A occurs before B.



[9 marks]

c) Consider the following given code segment:

```
loop: LW    R1, 0(R2)
      ADDI  R1,R1,#1
      SW    R1, 0(R2)
      ADDI  R2, R2, #4
      SUB   R4, R3, R2
      BNEZ  R4, loop
```

Assuming the DLX pipeline with *a single-cycle delayed branch* and *forwarding* hardware, *schedule* the instructions in the loop including the branch delay slot. As a designer, you can reorder instructions and modify the individual instruction operands. Show the pipeline timing diagram.

[4 marks]

d) Briefly discuss TWO advantages and disadvantages of Shared Bus.

[6 marks]

Continued .....

Question 3

i) Define the term of initiation rate, convoy, chime and vector start- up time.

[8 marks]

b) Determine three factors that affect the vector execution time?

[3 marks]

ii) Consider the following code, which multiplies two vector that contain single precision complex values:

```
for (i=0; i<300; i++){
        c=re[i] =  a_re[i] * b_re[i] – a_im[i] * b_im[i];
        c=im[i] =  a_re[i] * b_im[i] + a_im[i] * b_re[i];
}
```

Assume that the processor runs at 700MHz and has a maximum vector length of 64. The load/store unit has a start-up overhead of 15 cycles; the multiply unit, 8 cycles; and the add/subtract unit, 5 cycle.

iii) Calculate the arithmetic intensity of this kernel? Justify your answer.

[2 marks]

iv) Assuming chaining and a single memory pipeline, how many chimes are required?

[4 marks]

v) If the vector sequence is chained, how many clock cycles are required per complex result value, including overhead?

[2 marks]

e) A computer architect needs to design the pipeline of a new microprocessor. She has an example workload program core with 10^6 instructions. Each instruction takes 100 ps to finish.

i) How long does it take to execute this program core on a nonpipelined processor?

[2 marks]

ii) The current state-of-the art microprocessor has about 20 pipeline stages. Assume it is perfectly pipelined. How much speedup will it achieve compared to the nonpipelined processor?

[2 marks]

iii) Real pipelining isn't perfect, since implementing pipelining introduces some overhead per pipeline stage. Will this overhead affect instruction latency, instruction throughput, or both?

[2 marks]

Continued .....

Question 4

a) Briefly describe what is a Data Flow Graph and the definition of node in the data flow graph.

[4 marks]

b) Parallel communication is a method of conveying multiple binary digits simultaneously. List down and explains briefly the FOUR programming models of parallel framework for communication.

[8 marks]

c) Construct a data-flow graph for the following nested if-then-else statement.

```
if x > y then
        if k = i then
          z = a + b
        else
          z = c * d
else
        z = e + f
endif
```

[13 marks]

End of Paper